UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/557,520	01/30/2007	Minoru Ishikawa	00684.522762.	8818

5514 7590 11/13/2009

FITZPATRICK CELLA HARPER & SCINTO
1290 Avenue of the Americas
NEW YORK, NY 10104-3800

EXAMINER	
MOORAD, WASEEM	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
11/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/557,520	ISHIKAWA ET AL.	
	Examiner	Art Unit	
	WASEEM MOORAD	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al. (US 2003/0217871) in view of Yoshida et al. (US 5,798,756).

Regarding Claim 1, Chao et al. teaches a coordinate input apparatus, comprising:

A panel provided with a plurality of X interconnecting lines and a plurality of Y interconnecting lines disposed to intersect with each other in a matrix fashion (Figure 3)

Closed loop forming circuits disposed at two ends of the display panel (Figure 3 shows the ends of the display panel and shows the closed loop forming circuits),

Switching circuits connected to a terminal of each of the X and Y interconnecting lines (Figure 3, element 13);

A detection circuit for detecting signals outputted from the closed loop forming circuits in the coordinate detection drive mode in response to a position indicator for indicating a position in a coordinate input area of the panel where the X interconnecting lines and the Y interconnecting lines are disposed in the matrix fashion (Figure 3, element 10; section 0043-0046);

Wherein, in the coordinate detection drive mode, the closed loop forming circuits disposed at two ends of the display panel connect at least a pair of the terminals of the X interconnecting lines in each end to form a multiple closed loop as a closed loop circuit including multiple parallel loops of the X interconnecting lines and connect at least a pair of terminals of the Y interconnecting lines at each end to form a multiple closed loop of the Y interconnecting lines (Figure 3), and

The closed-loop forming circuits disposed at the ends of the display sequentially form multiple closed loops that are uniformly distributed with an embedded structure such that a multiple closed loop and another one subsequently formed overlap with each other (Figures 2-3)

Chao et al. does not teach a display panel provided with a plurality of X and Y interconnecting lines disposed to intersect with each other in a matrix fashion, display drive circuits for supplying drive signals to the X and Y interconnecting lines in a display drive mode, closed loop forming circuits disposed at opposite ends of each other and another two opposite ends of the display panel, and switching circuits connecting the X or Y interconnecting lines to the display drive circuits in the display drive mode and to the closed loop forming circuits in a coordinate detection drive mode.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chao et al. such that the closed loop forming circuits were also disposed at opposite ends and another two opposite ends of the display panel as an alternative design choice such that the odd X interconnecting lines could be connected with a pair of closed loop forming circuits, even X

interconnecting lines could be connected with a pair of closed loop forming circuits and the odd and even Y interconnecting lines could be connected with another pair of closed loop forming circuits, respectively.

Yoshida et al. teaches the coordinate input area is formed in a display panel (column 7, lines 16-30; where the panel is an LCD panel) and further teaches a circuit for switching a display drive mode using the matrix of the X and Y interconnecting lines and a coordinate detection drive mode using the matrix of the X and Y interconnecting lines (Figure 1, element 108; column 18, lines 19-25; where the changeover control circuit switches between the display driving circuit and the coordinate detection circuit).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chao et al. with the teachings of Yoshida et al. by having the coordinate input area formed in a display panel with a switching circuit between a display drive mode and coordinate detection mode, as well as the closed loop circuit operating the coordinate detection drive mode so the user can be given the option of looking at the display in the display drive mode or using the coordinate detection mode in order to determine the coordinates of a display panel (column 7, lines 32-36).

Regarding Claim 2, Chao et al. teaches wherein the closed loop includes a switch circuit for selecting first to four X interconnecting lines from the plurality of interconnecting lines (Figure 3) so that:

a first terminal of the first interconnecting line is connected with a first terminal of the second interconnecting line (Figure 3, where the first terminal is where the switches L1 open and close, and the first terminal of X1 connects to the first terminal (L2) of X2),

a first terminal of the third interconnecting line is connected with an output terminal (Figure 3, where the X3 line has L3 connected to the output nodes in element 13 that are directly below the switches and connected to the magnifying circuit 12), a second terminal of the third interconnecting line is connected with a second terminal of the first interconnecting line (Figure 3, where all the second terminals are have nodes in element 14, above the switches, and connect all the X first terminals together)

a first terminal of the fourth interconnecting line is connected with an output terminal (Figure 3, where the X4 line has L4 connected to the output nodes in element 13 that are directly below the switches and connected to the magnifying circuit 12), and

a second terminal of the fourth interconnecting line is connected with a second terminal of the second interconnecting line (Figure 3, where all the second terminals are have nodes in element 14, above the switches, and connect all the X first terminals together)

Chao et al. does not teach the third X interconnecting line located opposite to the first X interconnecting line with respect to the second X interconnecting line, and the first terminals of the even lines connected to the second output terminal)

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chao, in view of Yoshida, that when there are closed loop forming circuits on each end of the display and its divided into X-

odd, X-even, Y-odd, and Y-even, to have the X-even and X-odd interconnecting lines opposite to each other as an alternative design choice, which would then result in the first terminals of the odd lines connected to a first output terminal, and first terminals of the even lines connected to a second output terminal, rather than all the lines connected to one output terminal.

Regarding Claim 3, Chao et al. teaches wherein the closed loop includes a switch circuit for selecting first to four Y interconnecting lines from the plurality of interconnecting lines (Figure 3) so that:

a first terminal of the first interconnecting line is connected with a first terminal of the second interconnecting line (Figure 3, where the first terminal is where the switches L1 open and close, and the first terminal of Y14 connects to the first terminal (L2) of Y13),

a first terminal of the third interconnecting line is connected with an output terminal (Figure 3, where the Y11 line has L3 connected to the output nodes in element 13 that are directly below the switches and connected to the magnifying circuit 12), a second terminal of the third interconnecting line is connected with a second terminal of the first interconnecting line (Figure 3, where all the second terminals are have nodes in element 14, to the left of the switches, and connect all the Y first terminals together)

a first terminal of the fourth interconnecting line is connected with an output terminal (Figure 3, where the Y10 line has L4 connected to the output nodes in element

13 that are directly below the X switches and to the right of the Y switches and connected to the magnifying circuit 12), and

a second terminal of the fourth interconnecting line is connected with a second terminal of the second interconnecting line (Figure 3, where all the second terminals are have nodes in element 14, to the left of the switches, and connect all the Y first terminals together)

Chao et al. does not teach the third Y interconnecting line located opposite to the first Y interconnecting line with respect to the second Y interconnecting line, and the first terminals of the even lines connected to the second output terminal)

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chao, in view of Yoshida, that when there are closed loop forming circuits on each end of the display and its divided into X-odd, X-even, Y-odd, and Y-even, to have the Y-even and Y-odd interconnecting lines opposite to each other as an alternative design choice, which would then result in the first terminals of the odd lines connected to a first output terminal, and first terminals of the even lines connected to a second output terminal, rather than all the lines connected to one output terminal.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al. (US 2003/0217871) in view of Yoshida et al. (US 5,798,756) and further in view of Morita (US 5,128,499)

Regarding Claim 4, it is analyzed with respect to the analysis of Claim 1. Chao et al.., in view of Yoshida et al., is silent regarding wherein the closed loop is sequentially formed at a constant pitch on the matrix of the X and Y interconnecting lines with a lapse of time.

Morita teaches wherein the closed loop is sequentially formed at a constant pitch on the matrix of the X and Y interconnecting lines with a lapse of time (Figure 1, column 3, lines 65-68; where the closed loop has a constant pitch, element Ps)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chao, in view of Yoshida et al., with the teachings of Morita by having a closed loop formed at a constant pitch so to have equal conductivity between each of the sense lines on the X-Y matrix.

5. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al. (US 2003/0217871) in view of Yoshida et al. (US 5,798,756) and further in view of Kawai (US 2003/0086149)

Regarding Claim 8, it is analyzed with respect to Claim 1. Chao et al., in view of Yoshida et al., does not teach the display panel having a memory characteristic.

Kawai teaches an electrophoretic display having a memory characteristic (page 1, section 0003).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chao et al., in view of Yoshida

et al. with the teachings of Kawai by having a display panel having a memory characteristic so to have the ability to hold a display image (page 1, section 0003)

Regarding Claim 9, it is analyzed with respect to the analysis of Claim 8. Kawai further teaches the display panel being an electrophoretic display panel (page 1, section 0003).

Response to Arguments

3. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that the Oda reference in combination with Yoshida and Watanbe did not teach "...multiple closed loops as a closed-loop circuit consisting of multiple parallel loops of the X and Y interconnecting lines..." and that they don't "sequentially form multiple closed loops that are uniformly distributed with an embedded structure such that a multiple closed loop and another one subsequently formed overlap with each other"

Examiner fully considers and agrees with the Applicant's arguments. However, the arguments are moot in view of newly introduced reference: Chao et al.

Chao et al. teaches "...multiple closed loops as a closed-loop circuit consisting of multiple parallel loops of the X and Y interconnecting lines..." and that they don't "sequentially form multiple closed loops that are uniformly distributed with an embedded

structure such that a multiple closed loop and another one subsequently formed overlap with each other" (Figure 2 and Figure 3, element 14)

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WASEEM MOORAD whose telephone number is (571)270-3436. The examiner can normally be reached on M-F 730am-4pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Waseem Moorad/
Examiner, Art Unit 2629

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629

11/6/09